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# 可重构编码的低功耗16×16聚合物光开关阵列

周鸾宇[1],崔安琪[2],王祥宇[2],陈长鸣[2]
(1 国网黑龙江省电力有限公司尚志市供电分公司,哈尔滨 150600)
(2 吉林大学 电子科学与工程学院 集成光电子全国重点实验室,长春 130012)

**摘 要**:在低损耗氟化聚合物平台上设计并制备了16×16热光开关阵列。阵列器件由定向耦合-蜂窝网状单元器件级联而成,可通过热光调制实现256种开关状态切换。实际制备的器件尺寸约为7 cm×0.2 cm,在1 550 nm波长下,最低插入损耗为11.4 dB,最低开关功耗为33.38 mW,最大消光比为12.12 dB。在500 Hz调制频率下,实际测得器件的上升时间为226.7 μs,下降时间为294.0 μs;1 kHz极限调制频率下,上升时间和下降时间分别为222.2 μs和255.9 μs。研制的可重构低功耗16×16热光开关阵列,为光子集成与智能光调控提供了关键技术方案。该器件以其低功耗与可编程特性,有望推动数据中心光互连、光子神经网络及柔性可穿戴等系统的性能提升与架构革新,具备工程应用前景。

**关键词**:光电子学;聚合物光开关阵列;紫外直写;可重构编码;低功耗
**中图分类号**:TN256 **文献标识码**:A **doi**:10.3788/gzxb20265503.0355114

## 0 引言

在以人工智能、大数据和高性能计算为核心的数字化浪潮中,对信息处理容量与安全等级的需求日益提高[1]。传统电子集成电路在算力和能效方面面临着严峻的挑战,而集成光子技术,凭借光子固有的高带宽、低延迟及物理层安全特性,成为构建下一代通信系统的关键技术[2]。其中,可重构光网络是实现智能光计算与动态光加密的硬件基石,它允许在单个芯片上动态调制光信号的路径与功率,从而灵活适配多样化的算法与安全需求,为系统带来高灵活性与高效率[3-5]。然而,实现大规模、高密度的片上可重构光网络,其核心挑战在于功耗与集成度[6],而实现这样大阵列波导开关的主流平台仍是硅光和二氧化硅平台。目前,20信道,200 GHz的绝缘体上硅(Silicon-on-Insulator,SOI)波导波长选择开关已经成功研制,其平均插入损耗为29.6 dB,平均消光比为10.9 dB,其基于SOI波导高折射率对比度,可将器件尺寸控制在10 mm×5 mm,但其由于多波导互联和交叉及电极布线和调控不均问题,产生的相位误差和热串扰问题难以解决,这将直接导致其损耗和消光比均一性较差[7]。基于二氧化硅平台的11通道波长选择开关也被制备出来,其较低的折射率差可以很好地与光纤系统匹配,降低测试过程中的插入 损耗,其开关消光比可大于30 dB,插入损耗小于0.5 dB,串扰小于−14 dB,但由于二氧化硅材料的低热光系数限制,其单元开关功耗为360 mW,在高密度集成中面临性能和热管理方面的挑战[8]。传统基于SOI或二氧化硅的开关单元,其较高的开关功耗与热串扰问题,在阵列规模扩容时会急剧放大,成为制约系统规模与实用化的瓶颈[9,10]。此外,复杂的微纳工艺也提升了成本与集成难度[11]。

在此背景下,聚合物材料展现出了独特的优势,为破解上述难题提供了极具前景的解决方案[12]。聚合物材料拥有较高的热光系数,通常可比硅材料高出一个数量级[13]。这意味着,驱动相同的相位变化所需的功耗显著降低,为实现低功耗调制提供了物理基础。其次,聚合物是良好的热绝缘体,其低热导率特性能够

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**第一作者**:周鸾宇,zhouluanyu@163.com
**通讯作者**:陈长鸣,chencm@jlu.edu.cn
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有效将热效应局限在单个开关单元内，极大抑制了大规模阵列中邻近单元间的热串扰，保障了高密度集成的可行性与性能稳定性[14]。相较于无机材料，聚合物有着易于加工和改性的优势。其中氟代光刻胶以C-F键取代传统光刻胶波导材料的C-H键，显著降低材料在通信窗口（如1 550 nm）的光学吸收，是实现低损耗波导加工的关键。而有机无机接枝改性聚合物材料，则通过化学键将无机相的高热稳定性与有机相的良好成膜性、高热光系数和可调光学特性相结合，能大幅提升波导器件的环境稳定性、热稳定性并精确调控折射率，是制备高性能、高可靠集成光波导的理想选择。更为关键的是，聚合物波导器件通常采用旋涂、光刻与刻蚀等低温工艺，工艺复杂度相对较低，与互补金属氧化物半导体（Complementary Metal-Oxide-Semiconductor，CMOS）后端流程兼容性好，且原材料成本低廉[15]。这不仅有利于降低制造成本、提升制备效率，更便于在异质集成平台上实现与电子电路或其他光子功能模块的单片集成，为构建复杂多功能芯片铺平了道路[16]。

综上，本研究设计可重构编码的低功耗16×16聚合物光开关阵列，目的在于从器件层面为未来低功耗、高灵活度的智能光子系统提供一个可靠的硬件平台。其成功研制直接证明利用聚合物材料实现高密度、低功耗光路动态片上调制的可行性。以FSU-8作为波导的芯层材料，有机-无机接枝改性的聚甲基丙烯酸甲酯（Organic-Inorganic Grafting Polymethyl Methacrylate，OIG-PMMA）作为波导的包层材料，设计了低损耗、低功耗、高热稳定性的波导结构。在1 550 nm工作波长下，开关阵列器件实际测得具有11.4 dB的最低插入损耗，最低开关功耗为33.38 mW，最高消光比为12.12 dB。在500 Hz脉冲调制频率下，测得其上升时间为226.7 μs，下降时间为294.0 μs；在1 kHz极限调制频率下，上升时间为222.2 μs，下降时间为255.9 μs。与现有的大规模阵列波导开关相比，本研究低功耗、低损耗的特性可以满足便携化与高效调制的需求；其简单的工艺为低成本、规模化制造提供了方案；而其可重构能力，则是未来应用于智能光子加密系统的核心。

## 1 基本原理

### 1.1 DC-HC单元结构工作原理。

研究所采用的阵列波导开关由如图1(a)所示的单元结构定向耦合-蜂窝网状（Directional Coupler-Honeycomb，DC-HC）结构级联而成，在DC调制臂的一侧施加热光调制，可以实现功率交换功能。其中间HC区域引入相连的多段S型波导弯曲，可以满足127 μm的端口间距，且相并联的单元结构间可通过两个HC区域的相邻两臂之间形成DC结构，构建拓扑光网络。本研究中的DC-HC单元结构主要由两级DC及HC三部分构成。如图1(b)所示，当完全相同且相互平行的波导靠近时，因波导的模式耦合在波导间发生功率交换，这种现象称为定向耦合[17]。当一束沿$z$方向光耦合进入波导Ⅱ中时，两根波导之间的耦合系数$K$可以计算为

$$K=\frac{\gamma_1^2\gamma_2^2\exp\left(-\gamma_2 d\right)}{\beta k_0^2\left(n_1^2-n_2^2\right)\left(1+\gamma_2 a\right)} \tag{1}$$

其中

$$\begin{cases}\gamma_1^2=k_0^2n_1^2-\beta^2\\ \gamma_2^2=\beta^2-k_0^2n_2^2\\ k_0^2=\omega^2\mu_0\varepsilon_0\end{cases} \tag{2}$$

式中，$a$为波导宽度，$d$为两波导间的包层间距，$n_1$、$n_2$分别为芯层和包层的折射率，$\gamma_1$、$\gamma_2$分别为芯层和包层的横向衰减系数，$\beta$为模式传播常数，$k_0$为自由空间波数，$\omega$为角频率，$\mu_0$为真空磁导率，$\varepsilon_0$为真空介电常数。当波导长度$L$满足

$$L=(2m+1)\frac{\pi}{2K},(m=0,1,2,\cdots) \tag{3}$$

波导Ⅱ中的光功率完全耦合至波导Ⅰ，实现一次功率交换。

如图1(c)所示的HC结构是常用拓扑结构马赫-曾德尔干涉（Mach-Zehnder interferometer，MZI）的变形。是构建光调制器、光学开关、传感器以及可重构波长滤波器的关键单元[18]。在HC干涉结构中，输出信号光的强度和有效折射率变化量的关系为

$$I_{out}=|\Psi_0|^2\cos^2\left(\frac{\pi}{\lambda_0}\Delta n_{eff}L_M\right) \tag{4}$$

式中，$\Psi_0$为输入光的波函数，$\lambda_0$为信号光波长，$\Delta n_{eff}$为有限折射率变化量，$L_M$为调制臂的长度。

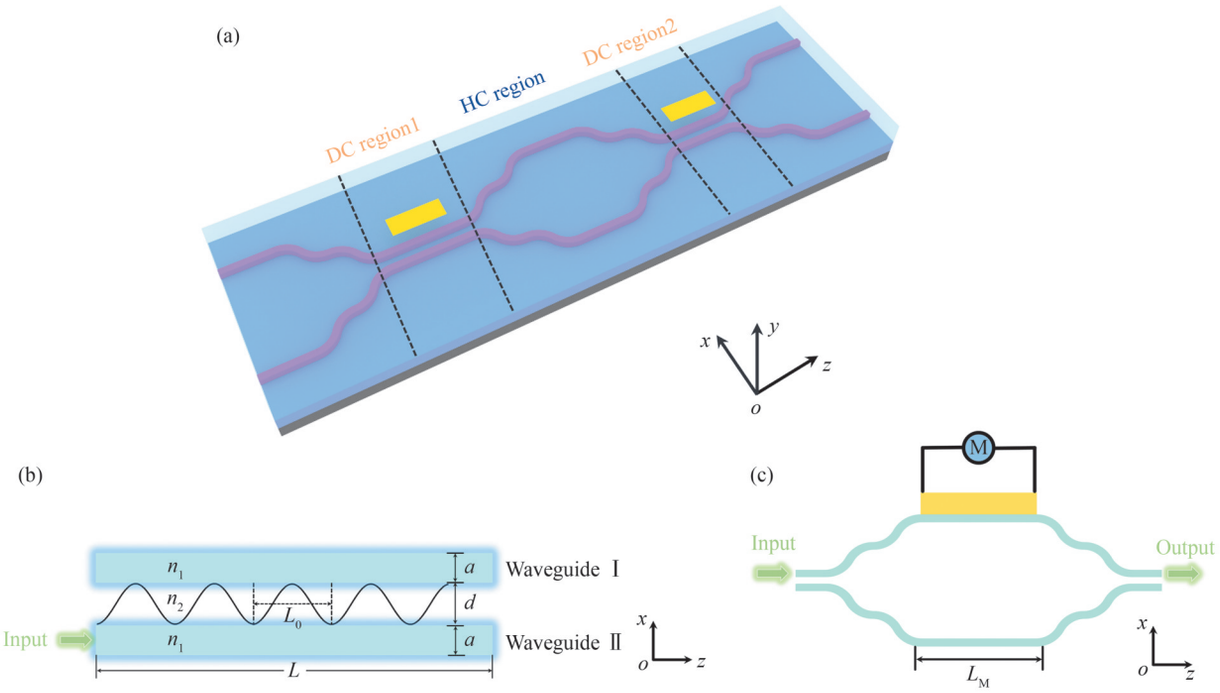


图1　器件结构示意。(a) DC-HC单元结构；(b) DC结构；(c) HC结构

Fig. 1　Schematic diagram of the device structure. (a) DC-HC unit structure; (b) DC structure principle; (c) HC structure principle

### 1.2　热光效应

热光效应是指材料折射率随温度变化的物理现象。聚合物光波导的热光系数($dn/dT$)通常为负值(约$-10^{-4}$/℃量级)，绝对值比硅等材料大一个数量级，这意味着其折射率对温度变化更敏感。结合聚合物固有的低热导率、易于加工等特点，使其成为实现低功耗、高调谐效率热光器件的理想平台。其响应速度通常在亚毫秒量级，适用于对速度要求不高但注重功耗和调谐范围的集成光子器件。其折射率变化量($\Delta n_{eff}$)随温度变化的表达式为

$$\Delta n_{eff}=-\frac{dn}{dT}\times\Delta T \tag{5}$$

式中，$\Delta T$为由电极加热产生的温度变化量，工作功耗$P$与温度变化量$\Delta T$的计算关系为

$$P=L_eW_eK_1\left(1+0.88\frac{H}{W_e}\right)\frac{\Delta T}{H} \tag{6}$$

式中，$L_e$、$W_e$分别为电极的长度和宽度，$K_1$为包层材料的导热系数，$H$为电极到波导芯层间距。

## 2　器件的仿真设计

为仿真可重构编码的低功耗16×16聚合物光开关阵列，本节应用光束传播法(Beam propagation method，BPM)，通过R-soft软件，针对单元结构和整体阵列结构分别优化了其传输和开关特性。研究采用的波导结构截面示意图如图2(a)所示，其中，硅衬底上生长的二氧化硅层的厚度$H_s$为5 μm，低损耗氟化光敏聚合物波导材料FSU-8作为芯层材料，芯层宽度$W_c$为3 μm，芯层厚度$H_c$为3 μm，铝电极宽度$W_e$为20 μm，电极与波导芯层间距$H$为3 μm，包层采用OIG-PMMA，厚度$H+H_c$为8 μm，该包层材料相较传统PMMA具有更高的热稳定性、自平整能力和相对高的热导率，有利于铝电极完美贴合在包层表面并降低功耗。两根定向耦合波导间距$W_g$为2 μm。在1 550 nm波长下，该波导结构$TE_{00}$模式$X-Y$截面光场如图2(b)，其有效折射率为1.51。如图2(c)所示，根据现有波导结构及其光、热学特性，模拟了其有效折射率随温度变化量之间

的关系曲线，计算得其有效折射率随温度变化的灵敏度为$-7.32\times10^{-5}$/K。为了减小波导的结构损耗，如图2(d)所示，优化的S弯$X$方向偏移量为63.5 μm，长度为1 000 μm，在该尺寸下，一个弯曲波导所带来的结构损耗约为0.014 dB，在进行开关阵列结构多段弯曲级联时，带来的结构损耗约为0.42 dB。如图2(e)所示，仿真的光纤-波导端面耦合损耗为3.455 dB/face，上述模拟结果对后续测试结果中的损耗分析提供了理论依据。

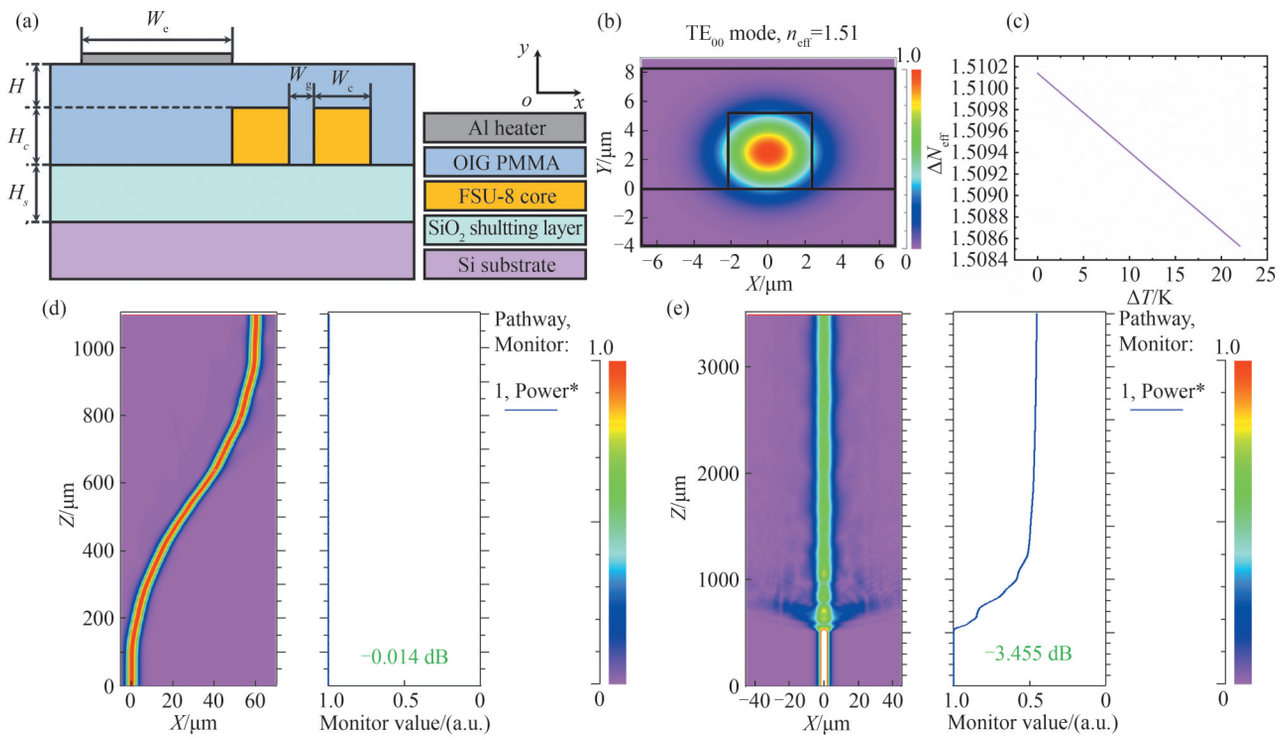


图2 器件的结构设计及波导损耗分析仿真。(a)波导的截面结构示意；(b)仿真计算的波导截面光场；(c)波导有效折射率随温度变化量关系曲线；(d)弯曲波导损耗分析；(e)波导-光纤耦合损耗分析

Fig. 2 Structural design and waveguide loss analysis simulation of the device. (a) Schematic of the waveguide cross-section; (b) Optical field simulation of the waveguide cross-section; (c) Relationship of waveguide effective refractive index versus temperature variation; (d) Simulation of bending waveguide loss; (e) Simulation of waveguide-fiber coupling loss

### 2.1 单元器件的设计

基于以上波导结构，设计的开关阵列的基本通道切换单元采用DC结构，应用铝电极作为加热电极附于DC调制臂的一臂左上方实现功率交换，其结构示意图如图3(a)。在现有波导尺寸和既定波导有效折射率条件下，仿真得DC结构耦合效率和耦合间距$W_g$的关系如图3(b)，当$W_g=2$ μm时，仿真获得的DC耦合效率接近100%，结合现有工艺条件，单元器件和阵列器件的耦合间距均设计为2 μm。如图3(c)所示，仿真了在耦合间距为2 μm时，耦合效率随耦合长度$L$的关系曲线，在$L=1\,631$ μm时，DC开关为cross态。如图3(d)所示，在铝电极上施加21 K的温差变化时，开关状态由初始的cross态切换为bar态，实现一次开关，理论计算得消光比大于35 dB，开关功耗小于32 mW。

在理论计算基础上，分别应用COMSOL Multiphysics软件中的有限元法(Finite Element Method，FEM)和R-soft软件中的BPM计算方法计算了该开关单元的$X-Y$截面热场和$X-Z$方向的光场传输。如图4(a)所示，当在DC单元左侧调制臂左上方的铝电极上施加21 K的相对温度变化时，通过添加热场等值线的方式更加清晰地给出热场仿真，距电极中心20～30 μm处热场已经完全退化成0 K，而相邻电极之间的距离约为172 μm，因此在阵列尺度下的温度场分布不会受热串扰的影响。通过仿真计算，在DC调制侧的另一臂波导中心处温度变化为0.22 K，根据$\Delta n_{\mathrm{eff}}=-\mathrm{d}n/\mathrm{d}T\times\Delta T$计算得，该波导臂的有效折射率变化量约为$-4\times10^{-5}$。而对阵列级器件的仿真方式是在阵列电极上施加温度场，因此实际仿真结果中已经考虑了DC非调制侧波导臂的有效折射率变化。至于相邻信道之间的串扰，仿真结果显示可大于30 dB。图4(b)、(c)分别为未施加/施加热调制时的DC开关单元的关/开传输光场仿真。

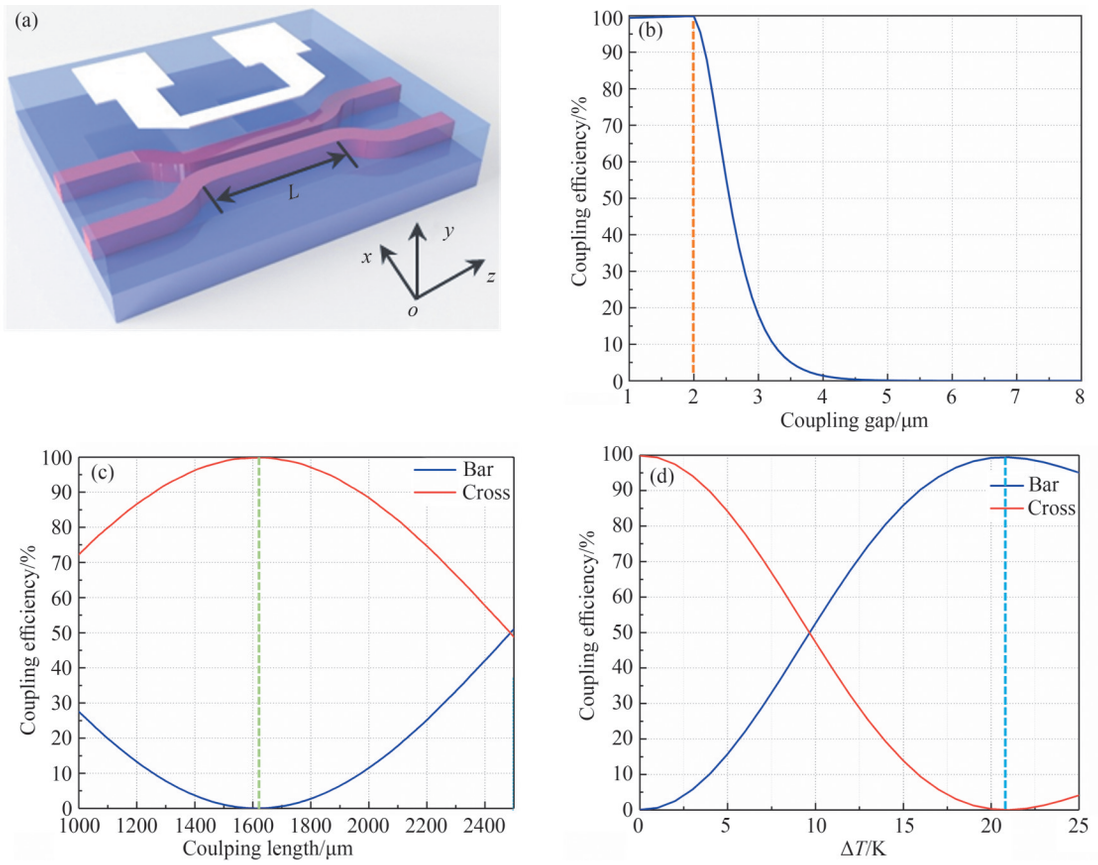


图3　DC开关单元结构示意及仿真。(a)DC开关单元结构;(b)DC耦合效率随耦合间距$W_g$的变化关系;(c)DC耦合效率随耦合长度的变化关系;(d)DC耦合效率随电极温度变化关系

Fig. 3　Structural dimension optimization of the DC switching unit. (a) DC switching unit structure; (b) DC coupling efficiency versus coupling gap $W_g$; (c) DC coupling efficiency versus coupling length; (d) DC coupling efficiency versus electrode temperature variation

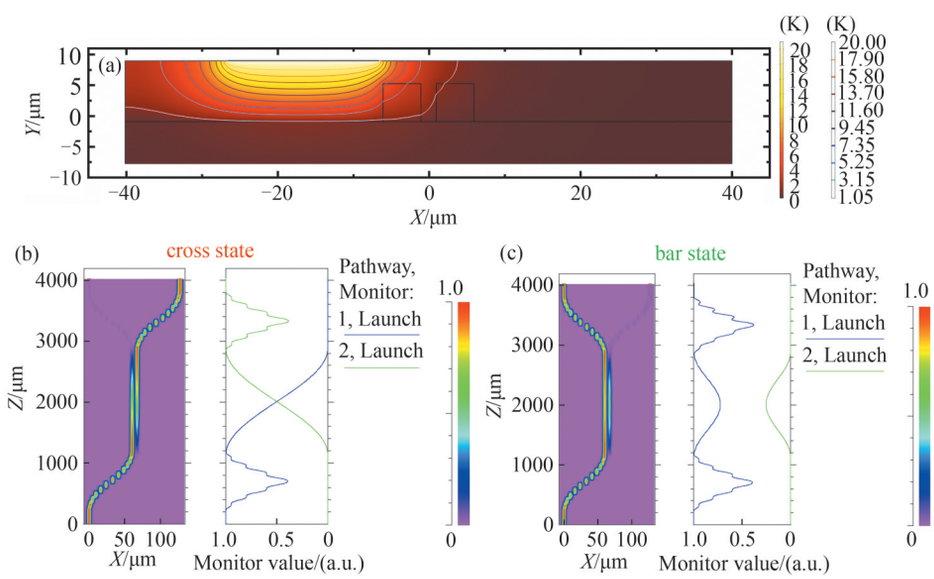


图4　DC开关单元光/热场仿真。(a)单元结构截面热场仿真;(b)交叉态光场仿真;(c)直通态光场仿真

Fig. 4　Optical/thermal field simulations of the DC switching unit. (a) Cross-sectional thermal field simulation of the unit structure; (b) Optical field simulation in the cross state; (c) Optical field simulation in the bar state

## 2.2　16×16开关阵列的优化仿真

如图5(a)所示,基于1.1节中DC-HC开关单元结构,16×16开关阵列的设计采用多组DC-HZ级联的形

式。开关阵列器件整体长度约为6 cm,宽度小于2 mm,相邻通道间距为127 μm,适用于与光纤阵列耦合,便于后续封装工作。设计15组蛇形电极,每组电极的宽度均设计为20 μm,可以实现对同一排所有DC开关同时调制。如图5(b)所示,由于篇幅受限,给出其以1通道输入,通过热电极调制可以任意实现1-16输出通道输出的光场仿真图。将以其他15个通道输入时的开关传输状态以真值表的形式附在了补充材料[19]中,真值表中的

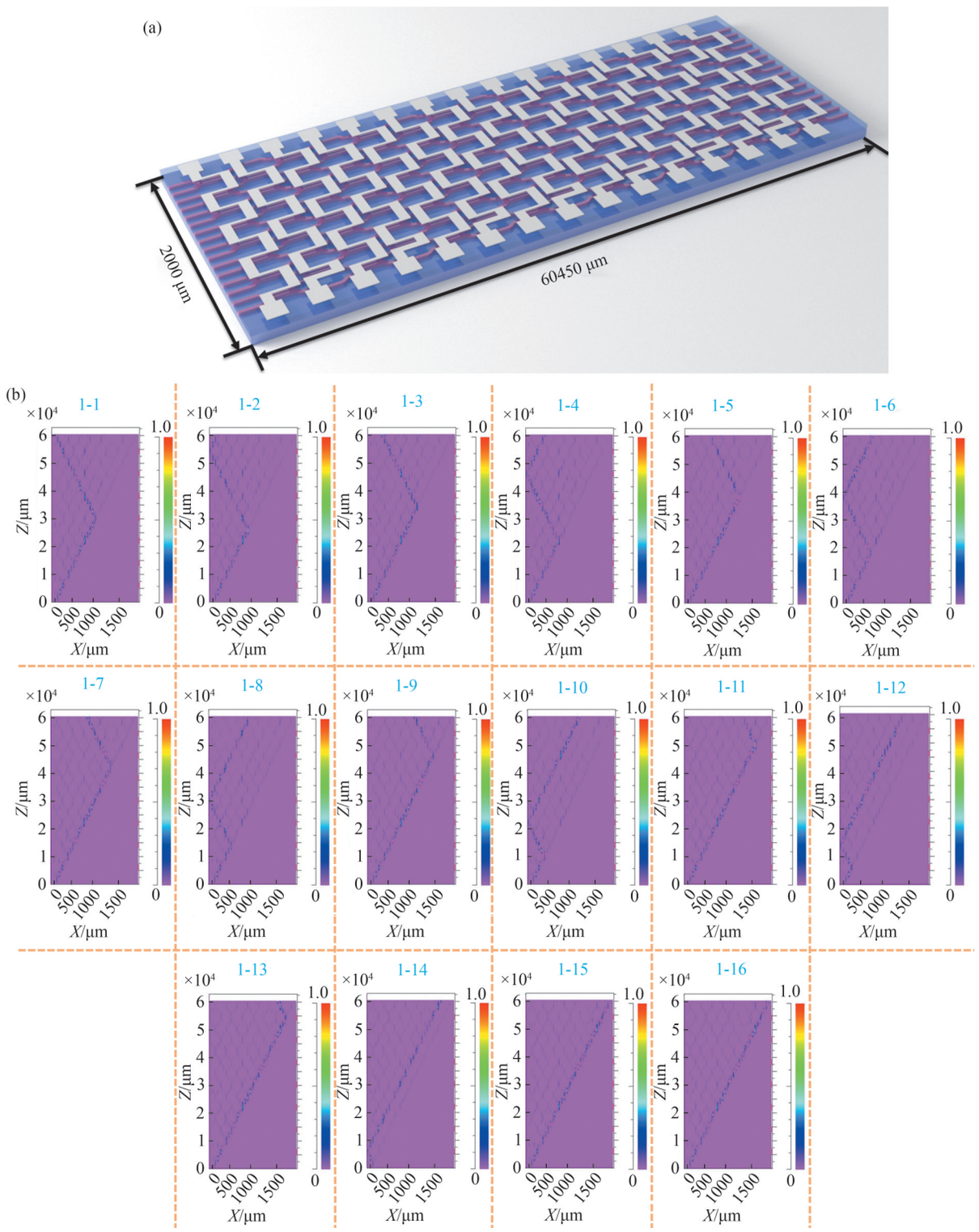


图5 开关阵列器件的结构示意和优化仿真。(a)开关阵列器件三维结构示意;(b)以1通道输入,经电极调制后1~16通道输出光场仿真示意

Fig. 5 Schematic and optimization simulations of the switch array device. (a) 3D schematic of the switch array device structure; (b) Simulation of the optical field output from channels 1 to 16 when channel 1 is input and modulated by electrodes

EX代表第X排蛇形电极，T1代表对开关阵列实际产生作用的电极，最右侧输出百分比为开关阵列器件经开关调制后对应输出通道的光功率百分比。作为示例，将获得的以1信道输入，1-16信道分别输出的透射率、累计损耗、相邻通道透射率和相邻通道间的串扰模拟结果体现在表1中。经计算，在1 550 nm波长下，其平均透射率、累计损耗、相邻通道透射率和相邻通道间的串扰分别为71.87%、1.58 dB、0.046%和－31.94 dB。

**表1　1信道输入，1-16信道分别输出的透射率、累计损耗、相邻通道透射率和相邻通道间的串扰模拟结果**

**Table 1　Simulation results of transmittance, cumulative loss, adjacent channel transmittance, and crosstalk between adjacent channels for outputs of channels 1-16 with 1 channel input**

| Channel | *T*/% | CL/dB | ACT/% | ACC/dB |
|---|---|---|---|---|
| 1 | 69.12 | 1.60 | 0.05 | －31.41 |
| 2 | 71.08 | 1.48 | 0.04 | －32.50 |
| 3 | 69.12 | 1.60 | 0.05 | －31.41 |
| 4 | 71.57 | 1.85 | 0.04 | －32.53 |
| 5 | 69.12 | 1.60 | 0.05 | －31.41 |
| 6 | 72.55 | 1.86 | 0.04 | －32.59 |
| 7 | 69.61 | 1.84 | 0.05 | －31.41 |
| 8 | 75 | 1.25 | 0.04 | －32.73 |
| 9 | 70.59 | 1.85 | 0.05 | －31.50 |
| 10 | 75 | 1.25 | 0.04 | －32.73 |
| 11 | 71.57 | 1.85 | 0.04 | －32.53 |
| 12 | 74.02 | 1.31 | 0.05 | －31.70 |
| 13 | 72.06 | 1.42 | 0.05 | －31.59 |
| 14 | 74.51 | 1.28 | 0.05 | －31.73 |
| 15 | 72.44 | 1.86 | 0.05 | －31.61 |
| 16 | 72.55 | 1.39 | 0.05 | －31.62 |
| Average | 71.87 | 1.58 | 0.046 | －31.94 |

*T*: Transmittance; CL: Cumulative loss; ACT: Adjacent channel transmittance; ACC: Adjacent channel crosstalk

## 3　器件工艺制备、表征及性能测试

### 3.1　器件的工艺制备及表征

本文的器件工艺制备方法采用标准FSU-8商用光刻胶的成熟工艺，OIG PMMA的合成及制备工艺和铝电极的制备工艺采用简单快捷的旋涂和湿法刻蚀[20, 21]。实际制备的器件的整体照片如图6(a)所示，其局部放

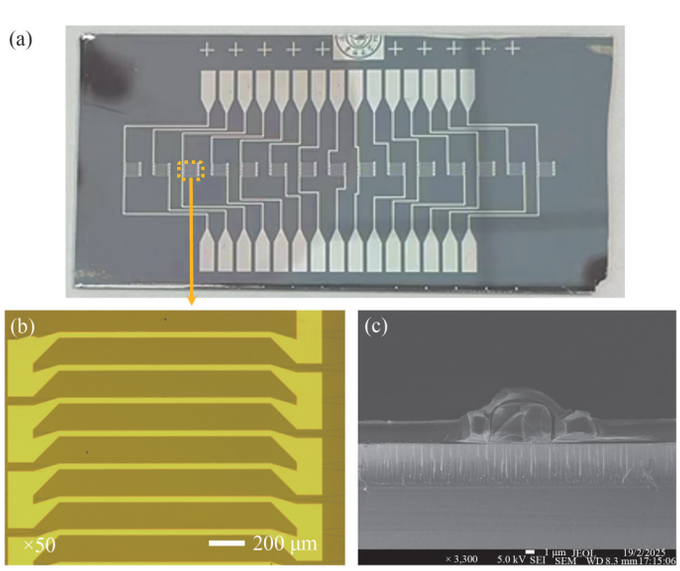


图6　开关阵列器件的实拍图像及电极、波导形貌表征。(a)器件实拍图；(b)器件电极部分局部放大显微镜表征；(c)波导端面结构SEM表征

Fig. 6　Physical images and characterization of the electrode and waveguide morphology for the switch array device. (a) Physical photograph of the device; (b) Microscopic characterization of a locally magnified area of the device electrodes; (c) SEM characterization of the waveguide end-face structure

大的蛇形电极结构如图6(b),实际制备的电极宽度约为21 μm,电极长度约为1 631 μm,尺寸基本符合预期。电极精准定位在DC调制臂的左上方,高精度的电极制备工艺是实现器件低功耗调控的关键。如图6(c)所示,波导端面的形貌方正,厚度约为5 μm,宽度约为6.2 μm,其中厚度符合预期仿真厚度,宽度相较设计波导宽度展宽1.2 μm。已经通过优化版图设计了从1到4 μm不等的容差,因此在3.2 μm耦合间距的器件版图设计中,制备出的耦合间距刚好为2 μm,这一间距与设计相符。精准的波导厚度使得器件的开关功耗符合预期,相对偏差较大的波导宽度可能会容纳更多高阶模式,模式色散会引起开关阵列器件通道间的串扰和影响单一通道消光比。

### 3.2 器件性能测试

分别就开关阵列器件开关性能进行静态和动态测试。如图7(a)、(b)所示,分别建立了静态开关性能和动态脉冲响应测试系统。在图7(a)中,1 550 nm波长连续信号光通过单模光纤(Single-Mode Fiber,SMF)连接在三环偏振控制器(Polarization Controller,PC)上,并通过端面耦合的方式耦合进入开关阵列芯片中,在对应的输出通道通过单模光纤输出至手持光功率计(Optical Power Meter,OPM)中读取损耗数据,记录好该通道初始数据后,通过直流稳压源输出电压,并通过一对探针分别加载在对应电极组的两端引脚上,以

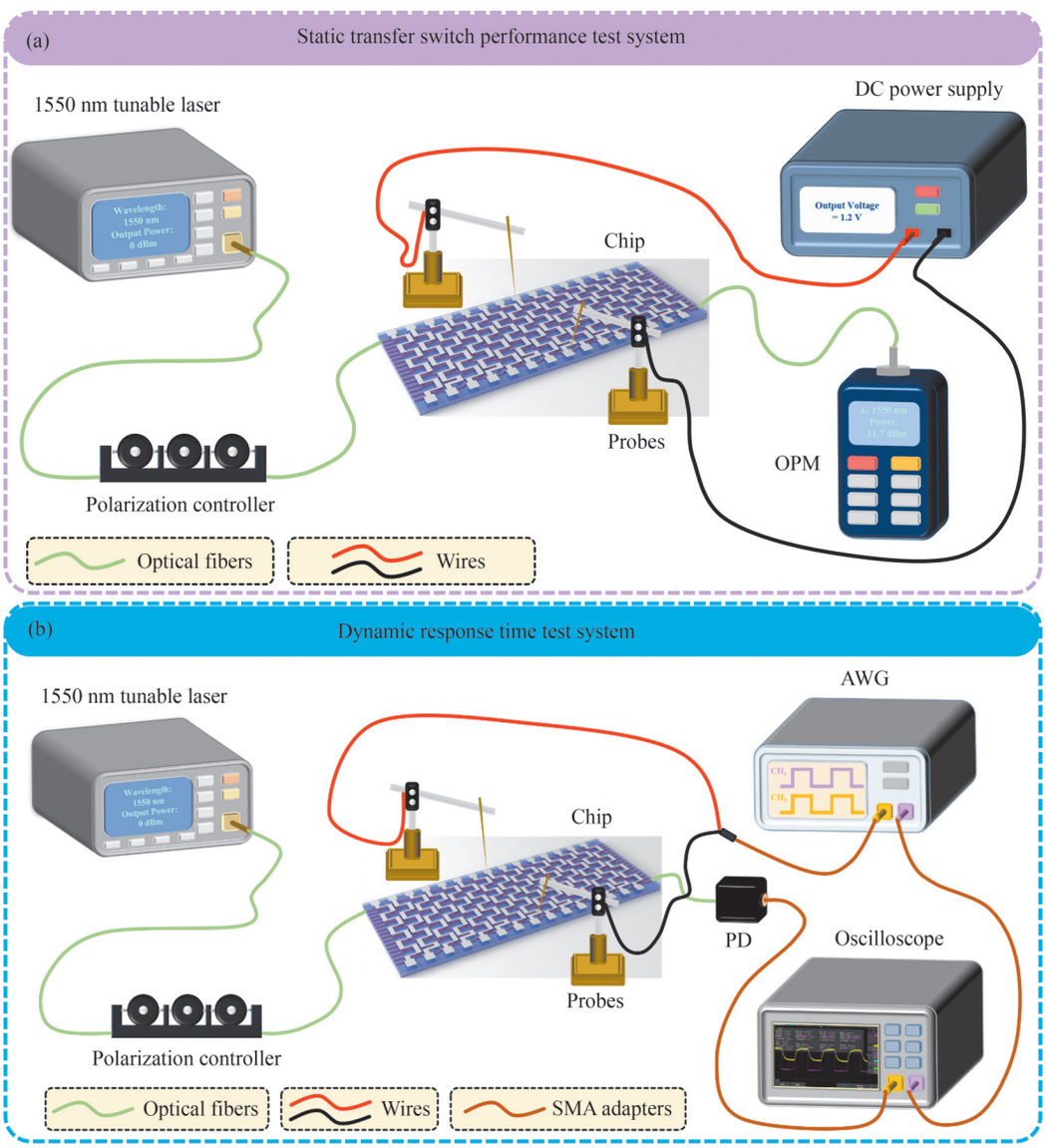


图7 器件测试系统示意。(a) 静态开关性能测试系统;(b)动态脉冲响应测试系统

Fig. 7 Schematic diagram of the device measurement setup. (a) Static switching performance test system; (b) Dynamic pulse response test system

0.2 V为电压增量，分别记录不同电压下该通道的插入损耗和工作功耗，完成该芯片的静态开关性能测试。在图7(b)中，仍以1 550 nm波长连续信号光和作为输入信号光，通过SMF和PC耦合进入波导芯片中，通过芯片后由一段SMF链接进入光电探测器(Photodetector，PD)中，将输出的光信号转换为电信号并通过小型射频同轴连接器(SubMiniature version A，SMA)连入示波器中获得信号光波形信号。然后采用任意波形发生器(Arbitrary Waveform Generator，AWG)，分别以500和1 000 Hz的脉冲频率从AWG的两个输出端口输出完全相同的两个脉冲信号，其中一路直接连入示波器中作为基准信号，另一路通过SMA)将对应的正负引线加载到对应通道的调制电极上，分别对比这两路脉冲信号，并记录在该调制频率下的响应时间，完成该芯片的动态脉冲响应测试。

实际制备的电极电阻约为145 Ω，根据电阻阻值，分别计算得如图8(a)～(d)所示的1信道输入，4、8、12、16信道分别输出的插入损耗随工作功耗的变化关系曲线。在1 550 nm工作波长下，该器件的最低插入损耗为11.4 dB，最大消光比为12.1 dB，同一通道开关状态切换的最小开关功耗为33.38 mW。通过仿真考虑由波导展宽带来的消光比退化和损耗估算。具体的仿真过程附在补充材料[22]中，计算得实际尺寸的DC-HC单元，由于波导展宽，其消光比退化为14.7 dB。开关阵列器件的插入损耗主要由结构损耗、端面耦合损耗和波导传输损耗三部分构成，其中，结构损耗约为1.51 dB，端面耦合损耗约为3.46 dB/face，波导材料传输损耗约为0.1 dB/cm，其余损耗归于波导解理面不平整和制备过程中由于波导粗糙度带来的散射损耗。

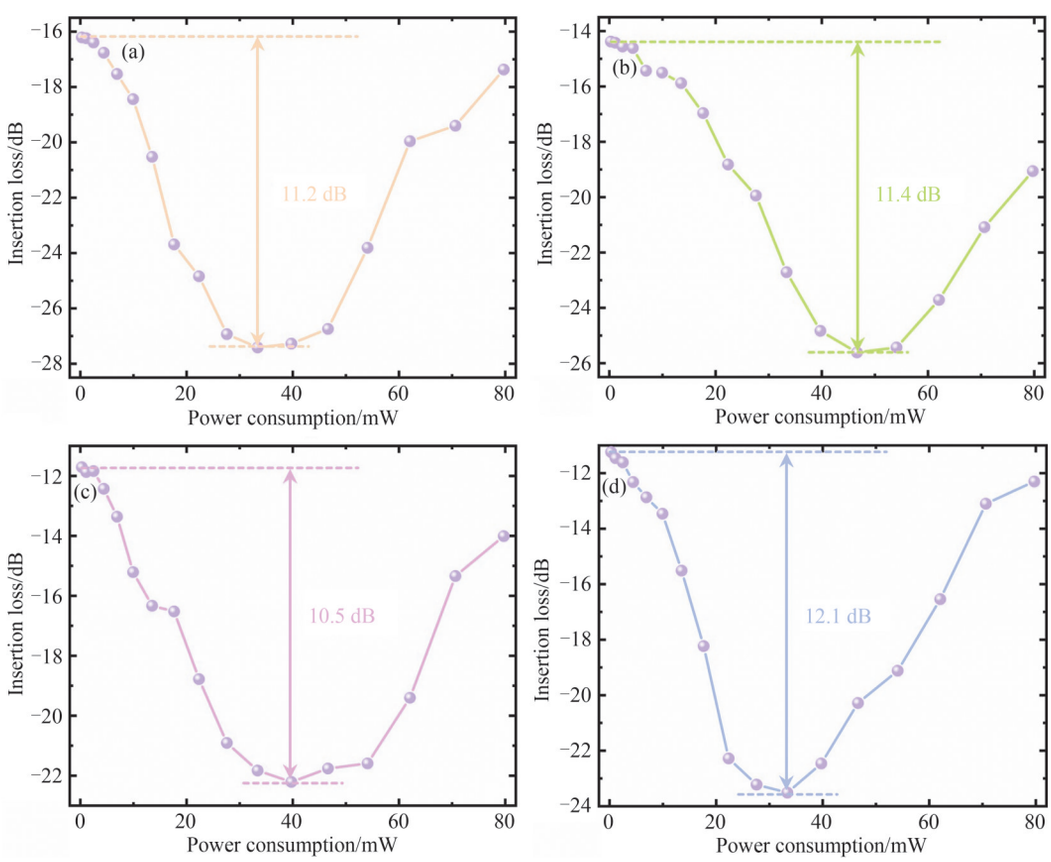


图8　器件静态开关性能测试结果。(a)1信道输入，4信道输出；(b)1信道输入，8信道输出；(c)1信道输入，12信道输出；(d)1信道输入，16信道输出

Fig. 8　Static switching performance test results for the device. (a) 1 input channel and 4 output channels; (b) 1 input channel and 8 output channels; (c) 1 input channel and 12 output channels; (d) 1 input channel and 16 output channels

利用脉冲响应测试系统，针对该器件的1通道输入、16通道输出进行其响应时间测试。如表2所示，在500 Hz调制频率下，实际测得该器件的上升时间和下降时间分别为226.7和294.3 μs。进一步对其工作极限频率测试，在1 kHz调制频率下，其上升时间和下降时间分别为222.2 μs和255.9 μs，且上升时间和下降时间的总和接近周期/2，认为器件工作性能勉强可用，因此定义该器件的极限调制频率为1 kHz。

表2 1信道输入,16通道输出响应时间测试结果

Table 2 Response time test results for 1-channel input and 16-channel output

| Working frequency/Hz | Rise time/μs | Fall time/μs |
|---|---|---|
| 500 | 226.7 | 294.3 |
| 1 000 | 222.2 | 222.2 |

表3为本研究的开关阵列器件与目前主流平台的量化性能对比,本研究的器件在16×16高集成度的工作能力下,其开关功耗相较于无机平台有明显优势,在端面耦合的测试方式下,其单位长度损耗最优,消光比优于部分无机平台,响应速度相对持平。后续的研究工作中,将会考虑以磨抛和点胶耦合的方式降低封装器件的插入损耗,提升开关阵列器件的通道均一性,通过电学封装提升系统稳定性和开关阵列的可编程、可重构能力,增大开关阵列规模,以期实现更高算力。本文所述聚合物平台满足CMOS后端的低温工艺预算,可通过通孔互连实现单片集成或采用2.5D封装。而大规模扩展至32×32或更高端口阵列时,将面临核心挑战:一是工艺上需保证器件性能的高度均匀性;二是热管理上必须解决密集有源器件间的热串扰问题。这为未来实现高密度光电集成的研究方向提供参考。

表3 不同平台开关/开关阵列器件性能对比

Table 3 Performance comparison of switch/switch array devices on different platforms

| Platform | Wavelength/nm | CC | PC/mW | PL/(dB·cm$^{-1}$) | ER/dB | RS |
|---|---|---|---|---|---|---|
| SOI[23] | 1 550 | 1×1 | 292.6 | 45.4 | 59.08 | 5.7 μs |
| Silica-polymer[24] | 1 310 | 1×1 | 8.72 | 31.08 | 18.64 | 184 μs |
| Silica[25] | 1 520~1 620 | 1×24 | 160 | 3.2 | 10 | 1.02 ms |
| Silicon nitride[26] | 532 | 1×2 | $P_\pi$= 0.63 | IL≈0.8 dB | 50 | 670 μs |
| LNOI[27] | 1 541.9 | 1×1 | $P_\pi$= 301 | — | 16.9 | 7.5 μs |
| Polymer[28] | 1 550.8 | 12×12 | 30 | 3.33 | 15.2 | 280 μs |
| This work | 1 550 | 16×16 | 33.38 | 1.63 | 12.12 | 226.7 μs |

CC: Channel count; PC: Power consumption; PL: Propagation loss; ER: Extinction ratio; RS: Response speed

如图9所示,依据本研究的波 导开关阵列,设定了跨城市贸易场景,以展示该器件在远距离数据中心信息动态加密领域的潜在应用。A市和B市两家贸易公司需在相距较远的数据中心间同步数据并发送指令,对延迟的敏感度达微秒级,且光纤存在被物理搭线窃听的风险。加密方法是,A市发出的商业数据在经数据中心处理后,可以输送至光加密芯片中,直接用高速密钥实时扰动光波的相位,在线路上传输密文噪声。在经长程传输接收端解密设备同步解密恢复原始信号,且对上层协议完全透明,再经数据中心将数据交付至B市,完成一套商业机密的加密和解密过程。这种物理层光加密为数据中心互联等高速场景在物理层面构筑防线,杜绝光纤窃听,同时以低延迟的透明方式运行,可实现商业机密保护。

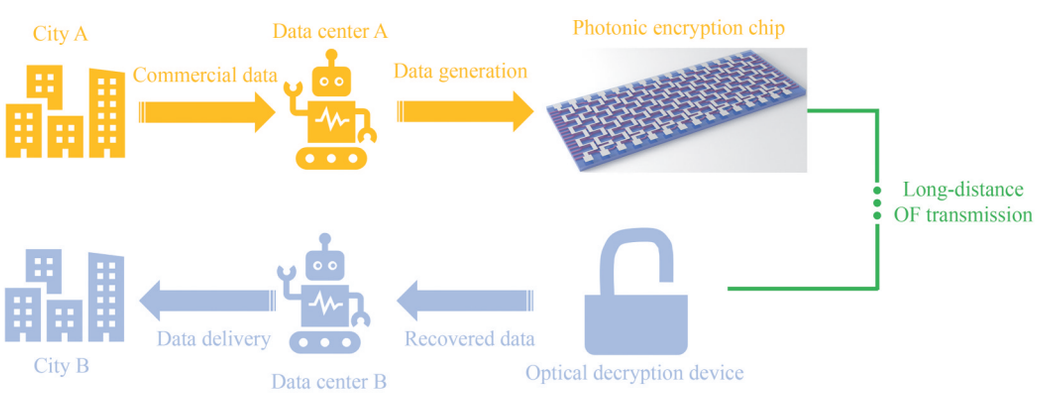


图9 波导开关阵列器件在远距离数据中心信息动态加密领域的应用场景示意

Fig. 9 Schematic application scenario of the waveguide switch array device in dynamic information encryption for long-haul data centers

## 4 结论

本研究采用低损耗氟化聚合物与有机-无机接枝改性材料体系,设计了基于DC-HC单元级联的可重构光开关阵列结构,实现了大规模、低功耗的光路动态切换与可编程功能。该工作有效解决了传统平台在阵列扩展时面临的高功耗、高损耗以及工艺复杂等关键问题,成功验证了聚合物材料在高密度集成光路调控中的独特优势。所研制的器件具备低功耗、高消光比与快速响应等综合性能,为智能光动态管理提供了可靠的硬件基础。该技术在数据中心光互连、光子神经网络、动态光加密以及柔性可穿戴光电系统等领域展现出广阔的应用前景。

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# Low-power Consumption Reconfigurable-encoded 16×16 Polymer Waveguide Switch Array

ZHOU Luanyu[1], CUI Anqi[2], WANG Xiangyu[2], CHEN Changming[2]
(1 *Shangzhi Power Supply Branch of State Grid Heilongjiang Electric Power Co., Ltd., Harbin* 150600, *China*)
(2 *State Key Laboratory of Integrated Optoelectronics, College of Electronic Science and Engineering, Jilin University, Changchun* 130012, *China*)

**Abstract**: This work aims to design, fabricate, and characterize a low-power, reconfigurable 16×16 thermo-optic switch array on a polymer-based photonic platform, addressing the critical challenges of high consumption and thermal crosstalk associated with scaling large-scale photonic integrated circuits. The primary goal is to develop a reliable hardware platform that demonstrates the feasibility of utilizing the unique material properties of polymers, specifically a high thermo-optic coefficient and low thermal conductivity for efficient and dense on-chip dynamic optical path control. The overarching purpose is to provide a foundational device solution to enable future low-power, flexible, and intelligent photonic systems for applications such as data center optical interconnects, photonic neural networks, and secure optical communications. The central research questions involve validating the performance metrics of a scalable polymer waveguide switch architecture and establishing its advantages over traditional inorganic platforms.

The study employed a comprehensive methodology integrating theoretical design, numerical simulation, process fabrication, and systematic experimental characterization. The core architectural innovation was the design of a cascadable unit cell termed the Directional Coupler-Honeycomb (DC-HC) structure, which combines a DC for power switching and a honeycomb HC interferometer for phase modulation. Multi-segment S-bend waveguides interconnect these units to achieve the required 127 μm port pitch for fiber array compatibility. A low-loss waveguide structure was meticulously designed and simulated. The core layer utilized a fluorinated photosensitive polymer, FSU-8, chosen for its low optical absorption at the 1 550 nm communication wavelength. The cladding material was an Organic-Inorganic Grafting Polymethyl Methacrylate (OIG-PMMA), selected for its enhanced thermal stability, self-planarization capability, and precise refractive index tunability. The optimized cross-section featured a 3 μm × 3 μm core, a 2 μm coupling gap between adjacent DC waveguides, and a 3 μm separation between the aluminum thin-film heater and the waveguide core. Beam Propagation Method (BPM) simulations using R-soft software were extensively conducted to optimize the waveguide geometry, including the DC coupling length, bending losses, and fiber-to-chip coupling loss. Finite Element Method (FEM) thermal simulations in COMSOL Multiphysics were performed to analyze heat distribution and cross-talk, confirming effective thermal confinement within individual switch units. Fabrication leveraged standard, cost-effective, and Complementary Metal-Oxide-Semiconductor (CMOS)-backend-compatible processes. The waveguide layers were defined through spin-coating, Ultraviolet (UV) lithography, and etching. Aluminum electrodes with a serpentine geometry were patterned via wet etching and precisely aligned atop the modulation arm of each DC unit. The fabricated devices were characterized using optical microscopy

and SEM to verify dimensional accuracy and morphology. A dual-system testing approach was implemented for performance evaluation. A static switching performance test system was constructed using a 1 550 nm continuous-wave laser source, a polarization controller, single-mode fibers for edge coupling, and an optical power meter. This system measured key static parameters: insertion loss and the required switching power consumption by applying a controlled DC voltage to the heaters. A separate dynamic pulse response system was built, incorporating an Arbitrary Waveform Generator (AWG), a Photodetector (PD), and an oscilloscope. This system measured the temporal response, specifically the rise and fall times, of the switches under square-wave modulation at frequencies of 500 Hz and 1 kHz.

The fabricated 16×16 polymer thermo-optic switch array exhibited compact dimensions of approximately 7.0 cm in length and 0.2 cm in width. Comprehensive testing at the 1 550 nm operational wavelength yielded a comprehensive set of performance data. The device achieved a minimum insertion loss of 11.4 dB. A detailed loss budget analysis attributed this to constituent factors: waveguide propagation loss, structural loss from cascaded bends, fiber-to-chip coupling loss, and additional scattering losses arising from fabrication imperfections such as sidewall roughness and imperfect cleavage planes. A core achievement was the demonstration of low-power operation. The minimum power required to toggle a single channel between its cross and bar states was measured to be 33.38 mW. This corresponds to applying a temperature change of approximately 21 K to the modulation arm, as predicted by thermal-optical simulations. The maximum extinction ratio achieved was 12.12 dB. While this value shows room for improvement compared to some inorganic platforms, it is attributed in part to a slight broadening of the fabricated waveguide width, which can support higher-order modes and introduce phase errors, as confirmed by supplementary simulations. Dynamic performance tests confirmed operation in the sub-millisecond regime. Under 500 Hz square-wave modulation, the measured rise time was 226.7 μs, and the fall time was 294.0 μs. When driven at a higher frequency of 1 kHz, the response times were 222.2 μs (rise) and 255.9 μs (fall), establishing this as the practical operational limit for the current device design. Simulation results for the full array predicted an average optical transmission of 71.87% and an adjacent channel crosstalk better than −31.94 dB for a signal routed from a single input to any output, indicating good routing fidelity. Crucially, thermal simulation results validated a key material advantage: the temperature field from an active heater decayed to ambient levels within 20～30 μm from its center. Given that adjacent switch electrodes are spaced approximately 172 μm apart, this confirms effective suppression of thermal crosstalk, a major bottleneck in densely packed inorganic switch arrays. A comparative analysis with state-of-the-art switches on platforms like silicon-on-insulator (SOI), Silica, and lithium niobate on insulator (LNOI) contextualizes the results. The polymer-based array demonstrates a compelling trade-off: its switching power is significantly lower than that of typical SOI or silica-based units, its unit-length propagation loss is advantageous, and its response speed is competitive with other polymer and hybrid systems. Most notably, it delivers this performance at a substantially larger port count, highlighting the scalability benefits of the polymer platform for large-scale photonic networks.

This research successfully validates the polymer material platform as a highly viable and competitive candidate for implementing scalable, low-power reconfigurable photonic integrated circuits. The developed DC-HC architecture and the associated fabrication methodology provide a concrete pathway toward constructing large-scale optical switching networks. The work conclusively demonstrates that the inherent material properties of polymers, specifically the high thermo-optic coefficient and low thermal conductivity, can be effectively harnessed to overcome key limitations of traditional platforms, namely high consumption and thermal crosstalk in dense arrays. The fabricated device, with its integrated combination of low switching energy, acceptable optical performance, microsecond-scale reconfigurability, and inherent programmability, establishes a significant hardware prototype. It serves as a critical enabling component for next-generation systems requiring dynamic optical path management. The findings are offering a practical device solution and a clear material and structural strategy for future work aimed at achieving even larger scale, lower loss, and higher-speed intelligent photonic processing systems.

**Key words**: Optoelectronics; Polymer optical switch array; UV direct writing; Reconfigurable-encoded; Low-power consumption

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